IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

KAIST IP US, LLC,	§	
	§	
Plaintiff,	§	
	§	
v.	§	No. 2:16-CV-01314-JRG-RSP
	§	
SAMSUNG ELECTRONICS CO., LTD., ET AL.,	§	
	§	
	§	
Defendants.	§	

CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER

On December 13, 2017, the Court heard argument on the proper construction of disputed claim terms in U.S. Patent 6,885,055. After full briefing and argument, the Court construes the disputed terms as set forth herein. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831 (2015).

Background

Plaintiff KAIST IP US, LLC has asserted the ’055 Patent against Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, LLC, GlobalFoundries, Inc., GlobalFoundries U.S. Inc., and Qualcomm Inc. The ’055 Patent relates generally to semiconductor manufacturing techniques for field effect transistors (FETs). ’055 Patent abst. More particularly, the ’055 Patent relates to the formation of a fin field effect transistor, also called a FinFET. *Id.*

The ’055 Patent describes reducing the transistor gate length as part of a drive to shrink

semiconductor devices and use less power. *Id*. at 1:20–37. But reducing the gate length of a traditional FET presents a number of performance issues. *Id*. at 1:30–64. Double-gate devices address these problems, and a FinFET is one such double-gate device that uses the sidewalls of a fin as the main channel regions. *Id*. at 3:24–29, fig.1c.

Legal Principles

A. Generally

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence, which includes the claims themselves, the specification, and the prosecution history. *Id.* at 1313–14; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"The claim construction inquiry . . . begins and ends in all cases with the actual words of the claim." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998). "[I]n all aspects of claim construction, 'the name of the game is the claim.'" *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298 (Fed. Cir. 2014) (quoting *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998)).

A term's context in the asserted claim can be instructive. *Phillips*, 415 F.3d at 1314. Other asserted or unasserted claims can also help determine the claim's meaning, because claim terms are typically used consistently throughout the patent. *Id.* Differences among the claim terms can also assist in understanding a term's meaning. *Id.* For example, when a dependent claim adds a

limitation to an independent claim, courts should presume the independent claim does not include the limitation. *See id.* at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id.* (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id.* (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *see also Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002).

But "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

The prosecution history can also supply the proper context for claim construction because, like the specification, it shows how the United States Patent and Trademark Office and the inventor understood the patent. *Phillips*, 415 F.3d at 1317. But "because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1318; *see also Athletic Alternatives, Inc. v. Prince Mfg.*, 73 F.3d 1573, 1580

(Fed. Cir. 1996) (noting ambiguous prosecution history may be "unhelpful as an interpretive resource").

Although extrinsic evidence can also be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises might help a court understand the underlying technology and the manner in which one skilled in the art uses claim terms, but they also might provide definitions that are too broad or not indicative of how the terms are used in the patent. *Id*. at 1318. Similarly, expert testimony might help a court understand the underlying technology and determine the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are entirely unhelpful to a court. *Id.* Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id.; see also Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015) ("In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period.").

B. Departing From the Ordinary Meaning of a Claim Term

Generally, courts give each claim term its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the patent. *Phillips*, 415 F.3d at 1312–13; *see also Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time.") (vacated on other grounds). There are, however, exceptions to that general rule, such as "1) when a patentee sets out a definition and acts as his own

lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution."[1] *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365 (Fed. Cir. 2014) (quoting *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)); *see also GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("[T]he specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal.").

The standards for finding lexicography or disavowal are "exacting." *GE Lighting Solutions*, 750 F.3d at 1309. To act as his own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term," and "clearly express an intent to define the term." *Id.* (quoting *Thorner*, 669 F.3d at 1365); *see also Renishaw*, 158 F.3d at 1249. The patentee's lexicography must appear "with reasonable clarity, deliberateness, and precision." *Renishaw*, 158 F.3d at 1249. To disavow or disclaim the full scope of a claim term, the patentee's statements in the specification or prosecution history must amount to a "clear and unmistakable" surrender. *Cordis Corp. v. Boston Sci. Corp.*, 561 F.3d 1319, 1329 (Fed. Cir. 2009); *see also Thorner*, 669 F.3d at 1366 ("The patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope."). "Where an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

[1] Some cases have characterized other principles of claim construction as "exceptions" to the general rule, such as the statutory requirement that a means-plus-function term is construed to cover the corresponding structure disclosed in the specification. *See, e.g.*, *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1367 (Fed. Cir. 2002).

C. Functional Claiming and 35 U.S.C. § 112, ¶ 6 (pre-AIA) / § 112(f) (AIA)[2]

A patent claim may use functional language. *See* 35 U.S.C. § 112, ¶ 6; *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347–49 & n.3 (Fed. Cir. 2015) (en banc in relevant portion). Section 112, Paragraph 6, provides that a structure may be claimed as a "means . . . for performing a specified function" and that an act may be claimed as a "step for performing a specified function." *Masco Corp. v. United States*, 303 F.3d 1316, 1326 (Fed. Cir. 2002).

But § 112, ¶ 6 does not apply to all functional claim language. There is a rebuttable presumption that § 112, ¶ 6 applies when the claim language includes "means" or "step for" terms, and that it does not apply in the absence of those terms. *Masco Corp*., 303 F.3d at 1326; *Williamson*, 792 F.3d at 1348. The presumption stands or falls according to whether one of ordinary skill in the art would understand the claim with the functional language, in the context of the entire specification, to denote sufficiently definite structure or acts for performing the function. *See Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1372 (Fed. Cir. 2015) (noting § 112, ¶ 6 does not apply when "the claim language, read in light of the specification, recites sufficiently definite structure" (quotation marks omitted) (citing *Williamson*, 792 F.3d at 1349; *Robert Bosch, LLC v. Snap-On Inc.*, 769 F.3d 1094, 1099 (Fed. Cir. 2014))); *Williamson*, 792 F.3d at 1349 (noting § 112, ¶ 6 does not apply when "the words of the claim are understood by persons of ordinary skill in the art to have sufficiently definite meaning as the name for structure"); *Masco Corp.*, 303 F.3d at 1326 (concluding § 112, ¶ 6 does not apply when the claim includes an "act" corresponding to "how the function is performed"); *Personalized Media Communications, LLC v. International Trade Commission*, 161 F.3d 696, 704 (Fed. Cir. 1998) (concluding § 112, ¶ 6 does not

[2] Because the application resulting in the '055 Patent was filed before September 16, 2012, the effective date of the AIA, the Court refers to the pre-AIA version of § 112.

apply when the claim includes "sufficient structure, material, or acts within the claim itself to perform entirely the recited function . . . even if the claim uses the term 'means.'" (quotation marks and citation omitted)). When it applies, § 112, ¶ 6 limits the scope of the functional term "to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson*, 792 F.3d at 1347.

Construing a means-plus-function limitation involves multiple steps. "The first step . . . is a determination of the function of the means-plus-function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). "[T]he next step is to determine the corresponding structure disclosed in the specification and equivalents thereof." *Id*. A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id*. The focus of the "corresponding structure" inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id*. The corresponding structure "must include all structure that actually performs the recited function." *Default Proof Credit Card Sys. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). Section 112, however, does not permit "incorporation of structure from the written description beyond that necessary to perform the claimed function." *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

For § 112, ¶ 6 limitations implemented by a programmed general purpose computer or microprocessor, the corresponding structure described in the patent specification must include an algorithm for performing the function. *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999). The corresponding structure is not a general purpose computer but rather the special purpose computer programmed to perform the disclosed algorithm. *Aristocrat Techs. Austl.*

Pty Ltd. v. Int'l Game Tech., 521 F.3d 1328, 1333 (Fed. Cir. 2008).

D. Definiteness Under 35 U.S.C. § 112, ¶ 2 (pre-AIA) / § 112(b) (AIA)[3]

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. A claim, when viewed in light of the intrinsic evidence, must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). If it does not, the claim fails § 112, ¶ 2 and is invalid as indefinite. *Id.* at 2124.

Courts decide whether a claim is indefinite from the perspective of one of ordinary skill in the art at the time the applicant filed the patent application. *Id.* at 2130. As it is a challenge to the validity of a patent, the failure of a claim to comply with § 112 must be shown by clear and convincing evidence. *Id.* at 2130 n.10. "[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012).

Not surprisingly, indefiniteness challenges frequently involve terms of degree and subjective terms. When a term of degree is used in a claim, "the court must determine whether the patent provides some standard for measuring that degree." *Biosig Instruments, Inc. v. Nautilus, Inc.*, 783 F.3d 1374, 1378 (Fed. Cir. 2015) (quotation marks omitted). Likewise, when a subjective term is used in a claim, "the court must determine whether the patent's specification supplies some standard for measuring the scope of the [term]." *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1351 (Fed. Cir. 2005); *accord Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014) (citing *Datamize*, 417 F.3d at 1351).

In the context of a claim governed by 35 U.S.C. § 112, ¶ 6, the claim is invalid as indefinite

[3] Because the application resulting in the '055 Patent was filed before September 16, 2012, the effective date of the AIA, the Court refers to the pre-AIA version of § 112.

if the claim fails to disclose adequate corresponding structure to perform the claimed functions. *Williamson*, 792 F.3d at 1351–52. The disclosure is inadequate when one of ordinary skill in the art "would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim." *Id.* at 1352.

Agreed Terms

Prior to the hearing, the parties agreed to the following constructions:

Term	Agreed Construction
a contact region and a metal layer which are formed at said source/drain and gate contact region (all asserted claims)	plain and ordinary meaning
a certain height (all asserted claims)	plain and ordinary meaning

J. Cl. Constr. Chart [Dkt. # 129-1] at 8, 21.

Disputed Terms

1. "a double-gate FinFET" (all asserted claims)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term does not need construction. The preamble is not limiting. If this claim term should be explicitly construed, then it should be construed under its plain and ordinary meaning in light of the specification as "a three-dimensional field-effect transistor device with a wrap-around gate structure."	The preamble is limiting because it is necessary to understand the scope of the claimed invention and should be construed under its plain and ordinary meaning as "a double-gate fin field-effect transistor device."

The Issues

The parties dispute whether the preamble limiting. If it is, the parties dispute the preamble's plain and ordinary meaning. Defendants limit the term to a FinFET with *only* two gates, while KAIST would include structures with more than two gates.

The Parties' Positions Concerning the Preamble as a Limitation

KAIST contends Defendants seek to limit the claim to a device with exactly two gates on the sides of the fin and exclude any embodiments that allow for an additional gate on the top of the fin. KAIST contends the preamble is not limiting and, even if it is, the claim language and specification expressly allow for more than two gates.

KAIST contends none of the terms found in the body of the claim depend on "double-gate" for antecedent basis support and the applicant placed no reliance on the preamble during prosecution. According to KAIST, the body of the claims provide a full and complete description of the invention and the preamble is not "necessary to give life, meaning, and vitality" to the claim because the limitations in the body of the independent claims recite the essential elements of a FET: "a Fin active region," "a gate," "a source/drain," and "a contact region and a metal layer which is formed at the source/drain and gate contact region." Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 3–4.

Defendants, on the other hand, contend the specification describes the "double-gate FinFET device" as the preferred and only embodiment and a core aspect of the invention. According to Defendants, "double-gate FinFET device" in the preamble gives life, meaning, and vitality to the asserted claims and informs the claim scope. Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 6–7 (citing cases).

Defendants note courts find preambles limiting where a term is repeatedly used throughout the specification to describe the invention. *Id*. (citing cases). Here, Defendants contend the specification repeatedly and consistently states the "present invention" provides or relates to a "double-gate FinFET device." Specifically, Defendants point to usages of "the present invention" in the Background of the Invention, Summary of Invention, and Abstract. Defs.' Resp. Cl. Constr. Br.

[Dkt. # 106] at 8 (citing ’055 Patent at 1:6–14, 4:10–19, abst.). Defendants further contend every embodiment in the specification describes a double-gate FinFET device. *Id.* at 8 (citing ’055 Patent at 4:10–11). “FinFET” appears 59 times in the specification, “double-gate” 29 times, and “double-gate FinFET” 12 times, including in the Title, the Abstract, the Background of the Invention, the Summary of the Invention, every embodiment, and every independent claim. Thus, in context of the specification as a whole, say Defendants, the preamble’s “double-gate FinFET device” gives life and meaning to the claims, providing essential structure to the claimed invention.

Defendants urge the Court to consider the preamble limiting because “absent construction of the preamble, the claims would be unbounded and could extend to structures well beyond the scope of the [asserted patent’s] specification.” Defs.’ Resp. Cl. Constr. Br. [Dkt. # 106] at 9. Failing to limit the claims to a “double-gate FinFET device” would improperly extend them to cover structures beyond what the patent contemplated. *Id*. at 9–10.

KAIST replies Defendants have not overcome the presumption that a preamble is not a claim limitation. For one, merely noting the preamble language appears in the specification fails to address the actual description. And here the actual description explains the double-gate FinFET device comprises a first oxide layer having a thickness greater than (no gate on the top) or equal to (additional gate present on the top) that of the gate oxide. Pl.’s Reply Br. [Dkt. # 113] at 2 (citing ’055 Patent at 4:28–31, 5:43–46, fig.9d). Based on the actual description, KAIST contends a person of ordinary skill in the art would understand the claimed invention includes a gate on the top of the fin *in addition to* the two necessary gates on the fin’s opposing sides. *Id*. at 2–3. KAIST emphasizes Defendants never define “double-gate,” and the patent never defines the term as a FinFET having exactly two gates. *Id*. at 3.

According to KAIST, Defendants' expert agreed the claim body recites all of the invention's necessary structural elements and the '055 Patent does not expressly disclaim an additional gate. Pl.'s Reply Br. [Dkt. # 113] at 3 (citing Subramanian Dep. [Dkt. # 93-3] at 81:24–82:13; *id.* at 295:6–8). KAIST reiterates that the specification expressly describes, and the claims cover, the embodiment of an *additional* gate on the top surface of the fin. *Id*. (citing Kuhn Decl. [Dkt. # 93-4] at ¶¶ 71–72).

As to Defendants' other preamble-related arguments, KAIST replies the claims are not "unbounded" because the express language in the body defines the invention. Defendants' argument of the preamble providing context for the invention is irrelevant, because all preambles provide claim context. KAIST again notes a preamble is not limiting unless it breathes life and meaning to the claims. Pl.'s Reply Br. [Dkt. # 113] at 3 (citing *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002)).

Finally, Defendants allege KAIST misrepresented a reference (Dr. Kuhn's own patent) as stating that the reference states that a double-gate FinFET may have a channel along the top of the fin. Defs.' Surreply [Dkt. # 117] at 1. Rather, the cropped language states the opposite:

presence of a third gate. Indeed, in the passage cited by Defendants of Dr. Kuhn's 2016 patent application, Dr. Kuhn refers to the "so-called" double-gate FinFET because the "conductive channel *principally* resides only along the two side-walls of the fin," not because it is *limited* to two side gates. Dkt. No. 106-16, at 1 (emphasis added). Thus, even in these later years, the terminology was context-dependent, and calling a device a double-gate FinFET did not necessarily exclude a gate on the top of the Fin. *Id.* Here, the context shows that the claimed double-gate FinFET is inclusive of a wrap-around gate on all three sides of the Fin, which allows for the presence of a gate on the top of the Fin.	Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).
Pl. Reply Br. at 6 (annotated).	Dkt. No. 106-16 ¶ 1 (U.S. Patent Appl. Publ. No. 2016/0276347 to Kuhn at al.) (annotated).

Id.

Analysis

"In general, a preamble limits the invention if it recites essential structure or steps, or if it is "necessary to give life, meaning, and vitality" to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 239 F.3d 801, 808 (Fed. Cir. 2001). "Conversely, a preamble is not limiting "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." *Id.* "When limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003). "When reciting additional structure or steps underscored as important by the specification, the preamble may operate as a claim limitation." *Catalina*, 239 F.3d at 808. Further,

> [c]lear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention. Without such reliance, however, a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention. Thus, preamble language merely extolling benefits or features of the claimed invention does not limit the claim scope without clear reliance on those benefits or features as patentably significant.

Id. at 808–09 (citations omitted). Finally, "preambles describing the use of an invention generally do not limit the claims because the patentability of apparatus or composition claims depends on the claimed structure, not on the use or purpose of that structure." *Id*. at 809.

Defendants have not shown the preamble should be limiting. First, the claims recite a structurally complete invention without reference to the preamble. The claims call out all necessary elements of a FinFET, including a fin active region, gate oxides on both side-walls of the fin active region, an oxide on top of the fin active region, a gate formed on the oxides, source/drain regions

formed in the fin active region, and a contact region at the source/drain and gate regions. Defendants have not identified any missing elements that render the body of the claim structurally incomplete.[4] This conclusion is not surprising given the Detailed Description describes the structure while never using the term "double-gate" except in a concluding paragraph.

Second, Defendants' argument that the preamble is limiting because the specification as a whole requires the claims to be limited to a structure that *only* uses two gates conflicts with the intrinsic evidence. The Background of the Invention first describes that a double-gate device "comprises" gate electrodes on two sides. '055 Patent at 2:1–3. Then the specification describes that the "double-gate device uses the etched vertical surfaces on both sidewalls of the body as the *main* channel regions." *Id*. at 3:27–29 (emphasis added). Defendants' interpretation ignores the explicit use of "main" (which implies there could be other channels) and re-writes "main" to mean "only."

More importantly, Defendants' position excludes a preferred embodiment, which "is rarely,

[4] At the hearing, Defendants argued the preamble is needed to understand that the claim is directed to a fin structure and the "a Fin active region" finds its antecedent basis in the term "FinFET" in the preamble. H'rg Tr. (Dec. 13, 2017) [Dkt. # 161] at 24–25. Defendants specifically argued the limitations of the body of the claim were solely directed to a general purpose FET. *Id*. at 25–26.

That position lacks merit, and the Court rejects Defendants' attempt to misread KAIST's expert's declaration as supporting such a position. The claim explicitly recites "a Fin active region," that the Fin active region is "wall-shape," a gate oxide on the "sidewalls of the Fin active region," and source/drain regions "formed on both sides of the Fin active region." The intrinsic and extrinsic evidence is devoid of any teaching that such structures are found in traditional planar FETs.

As to Kuhn's expert declaration, the paragraph cited by Defendants makes clear that when Kuhn noted the claim included "a Fin active region," Kuhn was referencing the "active region" part of the language as being an essential element of a FET. The very next sentence, for example, states "[a] FET is a transistor that has a gate, a source, a drain, a channel . . ." without reference to Fins, merely referencing source and drain which are active regions. Kuhn Decl. [Dkt. # 93-4] at ¶ 62. Defendants, however, completely ignore the rest of Kuhn's declaration and the extensive discussion of conventional planar FETs. *See id.* at ¶¶ 28–38.

if ever, correct." *See Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F.3d 1318, 1326 (Fed. Cir. 2013). The Detailed Description describes Figures 9a–9d as showing "the body structure of the FinFET device according to the first embodiment of the present invention." '055 Patent at 5:13–15. "FIG. 9d shows a cross section after growing a gate oxide layer 12 with a thickness between 0.5 nm and 10 nm in the formed Fin active region 4." *Id*. at 8:34–46. Layer 12 surrounds the Fin active region on the sides *and on the top*. *Id*. fig.9d. The gate region is formed on this structure. *Id*. at 8:43–46. Such an embodiment includes a top channel region in addition to the sidewall channel regions. Defendants contend such top channel regions are excluded from its understanding of "double-gate," *see* Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 10–14, but the teaching of a structure that provides three channel regions directly conflicts with Defendants' contention the totality of the specification is directed toward structures with *only* two channel regions. In short, this rejects Defendants' contention that to "give life, meaning, and vitality" to the claim the claimed structure must exclude any structure that includes a third channel.

Defendants counter it would not be known whether or not a channel is formed on the top of the fin active region in Figure 9d. H'rg Tr. (Dec. 13, 2017) [Dkt. # 161] at 32–35. Although Defendants acknowledged the oxide thickness impacts whether a channel is formed on the top surface of the Fin and all parties agree the thickness is a fundamental factor that affects channel formation, Defendants contended other properties—such as dielectric constant, doping of the fin active region, and the properties of the gate—would need to be known. *Id*. at 35. The intrinsic record, however, makes no mention of changing those other factors at the top of the fin active region to be different from the sides of the fin active region. Nor is there any teaching that the left, right and top of the fin are processed differently from each other. And when the issue was raised at the hearing as to why there would be a reason to believe Figure 9d intended the top to have

different variables, Defendants responded, "It's not clear." *Id*. at 34.

Based upon the totality of the intrinsic record, the Court finds Defendants' position requiring a strict negative limitation of no channel activity on the top of the fin active region conflicts with the intrinsic evidence. Moreover, as to the extrinsic evidence presented by the parties about the meaning of a "double-gate" at the time of the invention, the Court finds the evidence conflicting, and on the whole does not mandate excluding a top gate channel.[5] *See, e.g.*, Digh Hisamoto, *FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm*, 47 IEEE Transactions on Electron Devices No. 12 (Dec. 2000) [Dkt. # 93-19] at 2320; Kuhn Decl. [Dkt. # 93-4] at ¶¶ 38, 53, 77–78; [Dkt. # 93-10] at 124–25; Bokor Decl. [Dkt. # 93-12] at ¶¶ 55, 75; Subramanian Dep. [Dkt. # 93-3] at 59:2–6, 61:5–9, 75:80–13, 76:1–4, 100:3–10, 102:13–18, 102:23–103:13, 126:24–127:4, 128:14–20, 130:8–12, 132:19–24, 133:25–133:6, 142:8–14, 143:9–17; Park Dep. [Dkt. # 113-1] Ex. 3 at 53:9–12; Kuhn Dep. [Dkt. # 106-7] at 29:7–24, 31:5–23, 32:14–22, 34:8–12, 42:15–46:20, 49:22–50:25; [Dkt. # 106-16]; Kuhn Decl. [Dkt. # 93-17] Ex. M (Bokor Dep.) at 15:18–16:9, 69:25–70:12; Subramanian Decl. [Dkt. # 106-1] at ¶¶ 48–55; [Dkt. # 106-8] at 1:47–58, 3:16–4:13, 5:25–27; 2004 IEEE Si Nanoelectronics Workshop Program (June 13–14, 2004) [Dkt. # 106-22]. In the context of the totality of the extrinsic evidence discussed above, the Court

[5] Defs.' Sur-Reply [Dkt. # 117] attacks KAIST's expert's interpretation of the prior art. The Court, however, finds these references highlight the lack of clarity in the extrinsic evidence and contradict Defendants' contention that a "double-gate" cannot have channel regions other than the side channel regions. For example, as to the prior art figure pointed to in Kuhn's Declaration ¶ 38, the '055 Patent teaches a similar structure in Figure 9d and consistently refers to the structures of the patent as "double-gate." Yet the prior art references such a structure as a "triple-gate." Similarly, Kuhn's patent application refers to double-gate FinFETs in context of "the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin)." Defs.' Sur-Reply [Dkt. # 117] at 1. This reference makes clear that "double" is about where channels "*principally*" reside, not that there can be no channel on the top. Such references support the positions of KAIST.

thus finds the extrinsic evidence does not support the proposition that at the time of the invention "double-gate" had a meaning clearly known to exclude more than two gate channel regions. *See Teva Pharm. USA*, 135 S. Ct. at 841 (2015) (allowing courts to make subsidiary factual findings about the extrinsic evidence).

Although Defendants contend the entire specification is directed toward "double-gate" structures that do not have additional channel regions, the specification leaves room for debate about whether "double-gate" excludes any FinFET with three gate channels and whether "double-gate" excludes the "first embodiment" of the specification. Such debate contradicts Defendants' argument that the totality of the specification is directed toward FinFETs not having a third gate channel and contradicts any contention the term is needed to "give life, meaning and vitality" to the claims.

Given that, the Court concludes the preamble is not limiting.

* * *

2. "selective epitaxial layer is grown on both sides (source/drain region) of the Fin active region except where said Fin active region overlaps with the gate in a self-aligned manner to the gate" (claims 7, 9, 10, and 19)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term has a plain and ordinary meaning. No construction is necessary. If this claim term should be explicitly construed, then it should be construed under its plain and ordinary meaning in light of the specification as "selective epitaxial layer is grown on both sides (source/drain region) of the Fin active region except where said Fin active region overlaps with the gate *where the epitaxial layer is aligned relative to the location of the gate.*"	This claim element is a product-by-process limitation.[6] This claim term should be construed under its plain and ordinary meaning as "selective epitaxial layer is grown on both sides (source/drain region) of the Fin active region except where said Fin active region overlaps with the gate *in a manner aligned to the gate without the use of a lithography step."*

The Parties' Positions

The parties dispute the meaning of "self-aligned." The italicized portion of each party's proposed construction shows the competing meanings they give "self-aligned."

KAIST contends that in self-alignment, a pre-existing structure can be present that assists in the alignment process. For example, if a wooden plank is attached to a wall, and paint is applied to the wall on either side of the plank, the paint on the left and right sides of the plank can be described as self-aligned to the center of the plank. Pl.'s Opening Cl. Const. Br. [Dkt. # 93] at 10 (citing Kuhn Decl. [Dkt. # 93-4] at ¶ 84).

KAIST objects to Defendants' use of "without the use of a lithography step" as contradicting both the specification and the ordinary usage of "self-aligned." KAIST contends, as described

[6] For multiple terms, Defendants sought a ruling that a term is a product-by-process limitation. For now, the Court only addresses the construction of the disputed terms. The parties may raise the product-by-process issue in conjunction with any motion for which such issue is relevant.

in some embodiments of the specification, the gate is formed before the selective epitaxial step. *Id.* at 10 (citing '055 Patent at 6:47–49, 6:55–7:35). Moreover, "the gate 16 is defined by using photolithography." *Id.* (citing '055 Patent at 8:43–54, 9:27–38).

KAIST further contends the ordinary usage of self-aligned has contemplated the use of photolithography as part of a self-alignment process for decades. *Id.* at 10 (citing Kuhn Decl. [Dkt. # 93-4] at ¶¶ 84–88). As an example, KAIST notes a prior-art method of making transistor structures known as "tubs" that were "formed in a self-aligned manner" by using a "MASK 1." *Id.* at 10–11 (citing at Kuhn Decl. [Dkt. # 93-4] at ¶¶ 84–86; L.C. Parrillo, et al., *Twin-Tub CMOS—A Technology for VLSI Circuits*, Int'l Electron Devices Meeting (Dec. 8–10, 1980) [Dkt. # 93-20] at 752–55). KAIST argues masking patterns are common basic elements of photolithography used as part of self-alignment processes. *Id*. at 11 (citing Kuhn Decl. [Dkt. # 93-4] at ¶¶ 87–88).

According to KAIST, Defendants' negative limitation makes no sense because the presence or absence of photolithography does not determine whether a deposition process results in self-alignment. In fact, KAIST contends both parties' experts have confirmed the absence of lithography is not what determines whether selective epitaxial layer deposition is self-aligned. *Id*. (citing Kuhn Decl. [Dkt. # 93-4] at ¶¶ 90–92; Subramanian Dep. [Dkt. # 93-3] at 181:9–13).

Defendants, on the other hand, contend the '055 Patent teaches growing a selective epitaxial layer 18 on both sides of the fin active region 4. After forming the gate 16, an oxide is grown and etched to expose the source/drain areas of the fin active region 4. Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 18 (citing '055 Patent at 6:28–67, figs.5a & 5b). Defendants contend Figs. 5a–5b show the epitaxial layer 18 thickens the fin active region 4 on both sides of the gate 16, but that no epitaxial layer forms where the fin active region 4 overlaps with the gate 16.

According to Defendants, in MOSFET fabrication, a "self-aligned" process accomplishes

alignment without a lithography step. *Id*. at 18 (citing Subramanian Decl. [Dkt. # 106-1] at ¶ 81; Ben G. Streetman & Sanjay Banerjee, *Solid State Elec. Devices* (Prentice Hall 5th ed. 2000) [Dkt. # 106-18] at DEFTS_00000075; Peter Van Zant, *Microchip Fabrication* (McGraw-Hill 4th ed. 2000) [Dkt. # 106-19] at DEFTS_00000124).

As to KAIST's argument regarding the '055 Patent using a mask to form the gate, Defendants contend it is irrelevant whether the feature (i.e., the gate) to which the "selective epitaxial layer" is aligned is formed using lithography. Rather, what is relevant is whether a lithography step is used to align the "selective epitaxial layer" to the existing gate after formation. Defendants contend that, consistent with the plain meaning of "self-aligned," after gate formation, any later use of lithography to align the selective epitaxial layer to the gate defeats the **"**self-aligned" requirement in the claims. *Id.* at 18–19 (citing Subramanian Decl. [Dkt. # 106-1] at ¶¶ 84–87). Defendants contend KAIST's construction ignores the "self-aligned" requirement and interprets the element as if it merely recites "overlaps with the gate in an *aligned* manner to the gate."

KAIST replies Defendants merely argue the negative limitation is not inconsistent with the '055 Patent disclosure because there is no lithography step described as occurring after formation of the gate. KAIST contends (1) the mere absence of a description does not justify importing a limitation; (2) self-alignment and lithography are not mutually exclusive; and (3) lithography can be, and is, used as part of a self-alignment process. KAIST contends its construction makes clear the formation of the epitaxial layer relative to the location of the gate makes the process self-aligned, which is the ordinary understanding of this term. Pl.'s Reply Br. [Dkt. # 113] at 6–7.

Analysis

Defendants' only support for the inclusion of a negative limitation is that the '055 Patent does not disclose the use of a photolithography masking step between gate formation and growth

of the epitaxial layer. At the hearing, Defendants emphasized they were not attempting to exclude lithography from the process, but rather merely trying to give some meaning to "self-aligned." H'rg. Tr. (Dec. 13, 2017) [Dkt. # 161] at 50. But Defendants' construction is not so narrow.

As to the extrinsic evidence, the experts take competing positions as to the meaning of one skilled in the art and the interpretation of the extrinsic evidence, although the distinctions are subtle. Both sides agree that in a self-alignment process there is some step (e.g., a growth, a deposition, an etch) that occurs in some region on a substrate in which the alignment occurs in a self-aligned manner. But that does not necessarily mean other aspects of the self-aligned process do not use a lithography step, or even that other parts of the substrate are not lithographically masked in the same process step, while the location of intended "self-alignment" is left unmasked.

Defendants provide extrinsic references they contend show a "self-aligned" process accomplishes *alignment* without a lithography step. For example, Streetman describes not using a "separate lithography step," but does not state the use of lithography steps is excluded in a self-aligned process flow. Ben G. Streetman & Sanjay Banerjee, *Solid State Elec. Devices* (Prentice Hall 5th ed. 2000) [Dkt. # 106-18] at DEFTS_75. Van Zant describes "without the use of a photoresist alignment step." Peter Van Zant, *Microchip Fabrication* (McGraw-Hill 4th ed. 2000) [Dkt. # 106-19] at DEFTS_124.

The Court, however, finds these references do not stand for the use of no lithography steps. That some portion of the process occurs without a photoresist alignment step is different from Defendants' position in which there is no lithography step. For example, a lithography mask could block some portions of the substrate but leave open other areas for the self-aligned activity to occur.

In view of the extrinsic evidence and expert positions, KAIST's arguments are better supported. That there may be some self-aligned activity (e.g., a deposition, an etch, an implant) does not mean no lithography mask is used as part of the process. Thus, neither the intrinsic evidence nor the extrinsic evidence supports this negative limitation. This resolves the only dispute presented to the Court in connection with this term. The Court therefore construes "selective epitaxial layer is grown on both sides (source/drain region) of the Fin active region except where said Fin active region overlaps with the gate in a self-aligned manner to the gate" to have its plain and ordinary meaning.

* * *

3. "chamfered" (claim 15)

KAIST's Proposed Construction	Defs.' Proposed Construction
beveled or rounded	beveled

The Parties' Positions

The parties dispute whether "chamfered" corners can be "rounded." KAIST contends a person of ordinary skill in the art would understand chamfering encompasses a rounded corner. Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 11–12 (citing Kuhn Decl. [Dkt. # 93-4] at ¶¶ 168–71; Bokor Decl. [Dkt. # 93-12] at ¶ 130). KAIST contends Defendants' IPR expert explicitly stated as much and never made his construction contingent on the BRI standard applicable in IPR proceedings. Bokor Decl. [Dkt. # 93-12] at ¶¶ 35, 130. Moreover, Samsung's engineer admitted that its fin corners, which are rounded, are "chamfered." Pl.'s Reply Br. [Dkt. # 113] at 7 (citing Jeong Dep. [Dkt. # 113-1] Ex. 6 at 21:3–7).

Defendants contend "chamfered" should be construed as "beveled." Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 19 (citing *Am. Heritage Dictionary* (Houghton Mifflin Co. 4th ed. 2000)

[Dkt. # 106-20] at DEFTS_00000138 (defining chamber as "to cut off the edge or corner of; bevel")). The term only appears in one other place in the patent, which provides no guidance as to its meaning. *Id*. (citing '055 Patent at 6:4–8). As a result, Defendants contend KAIST cannot point to any figure or passage in the '055 Patent to support its construction. Defendants also complain KAIST does not cite any dictionary or technical treatise, and that Plaintiff merely points to a statement made in an IPR proceeding where claim terms are to be interpreted under the broadest reasonable interpretation standard.

Analysis

On balance, the extrinsic evidence supports KAIST's position that, as known in the semiconductor art, "chamfered" includes rounded corners. First, even Defendants' extrinsic evidence provides a potentially broader meaning than merely "beveled": "to cut off the edge or corner of." *See Am. Heritage Dictionary* (Houghton Mifflin Co. 4th ed. 2000) [Dkt. # 106-20] at DEFTS_00000138. Further, Dr. Kuhn states one skilled in the art would include rounded corners in the term's meaning because sharp corners rarely result in the nanometer dimensions at issue. *See also* Kuhn Decl. [Dkt. # 93-4] at ¶¶ 168–71 (citing other extrinsic evidence).

Likewise, Defendants' IPR expert states that, based on the plain and ordinary meaning of the term, the term includes the scenario "in which the top two corners are rounded." Bokor Decl. [Dkt. # 93-12] at ¶¶ 130–31. As noted by Defendants, differing standards may exist in IPR, but here the parties merely dispute the plain and ordinary meaning of the term to one skilled in the art. Dr. Bokor's testimony thus has at least some relevance.

When considering all the extrinsic evidence, KAIST's position is more reasonable. *See Teva Pharm. USA*, 135 S. Ct. at 841 (2015) (allowing courts to make subsidiary factual findings

about the extrinsic evidence). The Court therefore construes "the two top corners . . . are chamfered" to mean "the two top corners are "beveled or rounded."

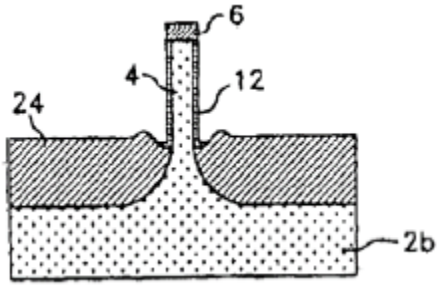
* * *

4. "trapezoid" (claim 14)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term should be construed under its plain and ordinary meaning in light of the specification as "shape wherein at least two opposing sides are not parallel, but which may include two other sides being parallel."	This claim term should be construed under its plain and ordinary meaning as "shape having two parallel sides."

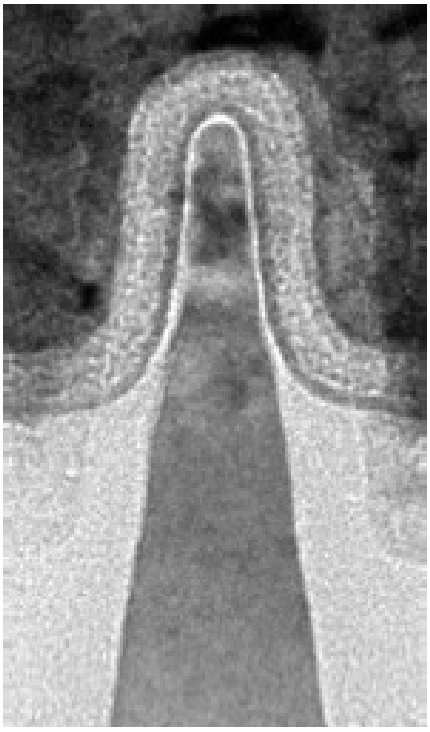
The Parties' Positions

The specification describes that the width of the fin active region is gradually increased such that "the shape of the Fin active region 4 can be a trapezoid where the width of the upper section is narrow and the lower section is wide." '055 Patent at 5:53–6:3. KAIST contends that, because of the varying width of the fin active region sides, and because they flare outward, the sides cannot be parallel as shown in Figure 13d:



'055 Patent fig.13d. KAIST contends Defendants' expert agrees this type of structure is a trapezoid. Pl.'s Opening Cl. Const. Br. [Dkt. # 93] at 12 (citing Subramanian Dep. (Oct. 23, 2017) [Dkt. # 93-3] at 43:2–21).

KAIST contends a person of skill in the art would have interpreted "trapezoid" in the context of a more rounded top surface because of the widespread existence of corner rounding in semiconductor fabrication. *Id.* at 12–13 (citing Kuhn Decl. [Dkt. # 93-4] at ¶¶ 174–75). Requiring geometric exactitude in the definition of "trapezoid" is inconsistent with how these structures exist in the real world. Accordingly, says KAIST, a person of ordinary skill in the art would know that in a "trapezoidal FinFET" the "triangular section is markedly different to the idealized rectangular section" of Figure 13d.



Id. (citing Peter Clarke, *Intel's FinFETs Are Less Fin and More Triangle,* EE Times (May 17, 2012) [Dkt. # 93-27]. KAIST contends Defendants' expert admits manufacturing tolerances in FinFET fabrication make it impossible to repeatedly create parallel lines. *Id*. (citing Subramanian Dep. [Dkt. # 93-3] at 204:23–205:25, 171:23–172:25). Thus, Defendants' requirement that the claimed

FinFET must have two parallel sides would effectively preclude any real world manufactured device.

KAIST contends its construction is meant to distinguish a trapezoid from, for example, a square or rectangle. KAIST states its extrinsic evidence shows a person of ordinary skill in the art would understand a "trapezoidal" FinFET to have a rounded top surface and no parallel sides—that is, closer to a triangular than a rectangle. Pl.'s Reply Br. [Dkt. # 113] at 7–8.

Defendants contend the plain and ordinary dictionary definition of "trapezoid" requires a "shape having two parallel sides." *See Am. Heritage Dictionary* (Houghton Mifflin Co. 4th ed. 2000) [Dkt. # 106-20] at DEFTS_00000142–143. Defendants contend there is no evidence the patentee redefined "trapezoid" from its plain meaning, and that KAIST ignores the basic requirement that a trapezoid has two parallel sides. Defendants contend their construction conforms to Figure 13d.[7] Moreover, the shape of the fin active region in Figure 13d is a "trapezoid" under Defendant's plain and ordinary proposal because "Fin active region 4" has two parallel sides as required under the plain and ordinary meaning of "trapezoid. Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 20.

Analysis

The parties do not dispute the ordinary meaning of trapezoid requires two parallel sides. Rather, KAIST expresses concern as to the meaning of "parallel" in a real-world product. *Id*. at 69–70. The only use of "trapezoid" in the specification does not indicate any lexicography or disavowal that contradicts the ordinary meaning. *See* '055 Patent at 6:1–3. Further, the parties agree

[7] The patent does not refer to the fin active region in Fig. 13d as a "trapezoid." Defendants, however, assume Fig. 13d is intended to show a "Fin active region" in the shape of a "trapezoid." Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 20 n.3.

Figure 13d is representative of the use of "trapezoid" in the specification. Figure 13d shows an example of a wider lower section. This figure also shows two parallel sides—the top and bottom—consistent with the patent's language. *See* '055 Patent fig.13d, 6:1–3. Such an interpretation of the two parallel sides of Figure 13d is also consistent with the plain and ordinary meaning of "trapezoid."

Although KAIST contends that rounding of corners is commonly known to occur in FinFET structures, and although KAIST cites a publication claiming some FinFETs may be "less Fin and more triangular" due to the geometries at issue, KAIST has not shown that merely because corners may round there can be no parallel sides. Furthermore, the intrinsic evidence does not suggest a redefinition of the term to include triangular-shaped structures. Finally, KAIST has not cited any lexicography, disavowal, or disclaimer redefining the term, and the intrinsic record is consistent with the plain meaning of the term. Therefore, the Court does not find evidence supporting redefining the term "trapezoid" to remove the parallel side aspect from the plain and ordinary meaning of the term.

For these reasons, the Court construes "trapezoid" to mean "a shape having two parallel sides."

* * *

5. "said first oxidation layer" (claims 1–6, 11, 12, and 14–17)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary, but if "first oxidation layer" should be explicitly construed, then it should be construed under its plain and ordinary meaning in light of the specification as "first oxide layer."	Indefinite

The Parties' Positions

The parties dispute whether "said first oxidation layer" is indefinite as lacking antecedent basis or whether the term refers to the earlier-recited "a first oxide layer."

KAIST contends the language and structure of the claim make clear "the first oxidation layer" refers to "a first oxide layer" earlier in the claim. The claims first recite "a gate oxide" and "a first oxide . . . with a thickness greater or equal to the gate oxide," and then recite the "thickness of said gate oxide layer is between 0.5 nm and 10 nm, and the thickness of said first oxidation layer is between 0.5 nm and 200 nm." KAIST contends the repetition of "first" and the concept of "thickness" expressly informs a person of skill in the art the "first oxide layer" is the "first oxidation layer." Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 18. KAIST also notes the specification's interchangeable use "first oxide layer 6" and the "first oxidation layer 6," '055 Patent at 10:24–34, "the second oxide layer 10" and the "second oxidation layer 10," *id*. at 7:6–15, 5:58–62, and "oxide" and "oxidation," *id*. at 6:50–59, 9:44–52. Finally, KAIST notes Defendants' expert had no trouble understanding the meanings of first oxidation layer, gate oxide layer, and their respective thicknesses when he testified about this claim term. Pl.'s Opening Cl. Const. Br. [Dkt. # 93] at 19 (citing Bokor Decl. [Dkt. # 93-12] ¶ 91).

Defendants, on the other hand, contend "oxidation layer" has no antecedent basis and, because "oxide layer" has a different meaning than "oxidation layer," has multiple different interpretations. Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 22. Both experts agree an "oxidation layer" is a "layer formed by oxidation." *Id*. Defendants claim "oxidation" is a well-known process whereby a material is exposed to oxygen to form an oxide. *Id*. (citing Subramanian Decl. [Dkt. # 106-1] ¶ 93; [Dkt. # 106-7] at 155:24–156:4; Peter Van Zant, *Microchip Fabrication* (McGraw-Hill 4th ed. 2000) [Dkt. # 106-19] at DEFTS_00000121). In contrast, a person of skill in the art would have

understood "oxide layer" to merely mean a "layer that is oxide"—not necessarily that the layer was formed by "oxidation." Defendants contend that, because "oxidation layer" and "oxide layer" have different meanings, a person skilled in the art would not understand to which layer "said first oxidation layer" refers.

As to Defendants' assertions that "oxidation layer" refers to a particular method of formation, KAIST replies the specification expressly refers to "oxidation layers" as deposited, which is contrary to Defendants' distinction. Pl.'s Reply Br. [Dkt. # 113] at 8 (citing '055 Patent at 9:31–33; Kuhn Decl. [Dkt. # 93-4] at ¶¶ 96–99).

Analysis

From the context of the claim, the "first oxidation layer" is "first oxide layer." This is clear from the claims' references to the "gate oxide" and the "first oxide layer," the relative thicknesses of the two, and then the claim's subsequent recitation of the layer thicknesses. Moreover, the specification repeatedly uses the terms interchangeably. *See* '055 Patent at 10:24–34, 7:6–15, 5:58–62, 6:50–59, 9:44–52. And though Defendants make much of an "oxidation layer" being a grown layer formed by oxidation, the specification explicitly references the "oxidation layer" as a layer that "is deposited." *Id.* at 9:31–33.

In light of the context of the claims and the specification as a whole, the Court construes "said first oxidation layer" to mean "said first oxide layer."

* * *

6. "the parasitic capacitance between said gate and bulk silicon substrate is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm" (claim 5)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary, but if "second oxidation layer" should be explicitly construed, then it should be construed under its plain and ordinary meaning in light of the specification as "second oxide layer."	Indefinite

The Parties' Positions

Defendants contend "reduced" is unclear because there is no indication as to the amount of reduction. Defendants further contend there is no baseline against which any reduction can be compared. Finally, Defendants claim "said second oxidation layer" lacks antecedent basis.

KAIST contends the meaning and scope of "parasitic capacitance" is a well-understood concept in the art and defined in the claim. As recited in the claim itself, the parasitic capacitance is between the gate and bulk silicon substrate. The specification teaches "the thickness of the second oxide layer 10 is selected in a range from 20 nm to 800 nm in order to reduce the parasitic capacitance between the gate 16 and bulk silicon substrate 2b." *Id*. at 20 (citing '055 Patent at 5:53–56).

KAIST cites Defendants' IPR expert for the well-known principle that parasitic capacitance is inversely proportional to the thickness of the isolation film 14. *Id*. (citing Bokor Decl. [Dkt. # 93-12] ¶ 105); *see also id.* (citing Subramanian Decl. [Dkt. # 106-1] ¶¶ 59, 61; Kuhn Decl. [Dkt. # 93-4] ¶ 112). KAIST contends selecting the lower limit of 20 nm means the resulting parasitic capacitance is reduced as compared to any thicknesses less than 20 nm, which sets the lower limit.

KAIST contends too thick of a second oxide layer presents problems (e.g., void-free deposition), which is why this particular embodiment caps the second oxide thickness at 800 nm. *Id*. at 20–21 (citing Kuhn Decl. [Dkt. # 93-4] ¶ 111–13). KAIST contends the claim permits decreasing parasitic capacitance by increasing the thickness of the second oxide layer above 20 nm with a ceiling at 800 nm. *Id*. at 21.

Defendants contend the requirements of the claim language produce different results that may or may not meet this limitation depending on the missing baseline reference. For example, if the thickness of the "second oxidation layer" in the baseline was greater than 800 nm, "selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm" would increase the parasitic capacitance. In contrast, if the thickness of the "second oxidation layer" in the baseline was less than 20 nm, "selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm" would reduce the parasitic capacitance. *Id.* at 23–24.

Defendants contend claims such as these—that is, those that require separate determinations of infringement at different times and under different circumstances—are indefinite. *Id*. at 24 (citing *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1255 (Fed. Cir. 2008) ("When a proposed construction requires that an artisan make a separate infringement determination for every set of circumstances in which the composition may be used, and when such determinations are likely to result in differing outcomes (sometimes infringing and sometimes not), that construction is likely to be indefinite.")).

Finally, Defendants claim the lack of antecedent basis for "said second oxidation layer" renders the term indefinite, providing arguments similar to that discussed above with regard to the "said first oxidation layer." *Id*.

Analysis

Regarding the "said second oxidation layer" dispute, the Court finds that, as with the "first oxidation layer" term, the intrinsic record makes clear the "said second oxidation layer" references the earlier recited "second oxide layer." The specification uses the "second" terms interchangeably. *See* '055 Patent at 5:48, 7:8–9, 5:58–62, 6:50–59, 7:6–15, 10:24–34. Further, the specification makes clear the second oxide affects the parasitic capacitance between the gate and the bulk silicon substrate. *Id*. at 5:53–56.

As to Defendants' argument the term is indefinite for not providing a degree of the amount of reduction, the argument fails because the term is not a term of degree. Rather, the claim merely requires a reduction in parasitic capacitance, not a specific amount of reduction.

Finally, Defendants contend there is no reference against which to compare the reduction in capacitance. All the experts agree, however, that it is fundamental and well-known that the capacitance reduces as thickness increases. *See* Kuhn Decl. [Dkt. # 93-4] ¶ 112; Bokor Decl. [Dkt. # 93-12] ¶ 105; Subramanian Decl. [Dkt. # 106-1] ¶¶ 59, 61. The claim clearly recites a desired range for the oxide thickness, and the specification describes this range as providing a reduced parasitic capacitance between the gate and the bulk silicon. '055 Patent at 5:54–57. Thus, one skilled in the art would understand that selection of a thickness in the recited range provides sufficient parasitic capacitance characteristics and the capacitance would be reduced compared to capacitance thicknesses less than that range—i.e., less than 20 nm.

For these reasons, the Court finds "the parasitic capacitance between said gate and bulk silicon substrate is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm" is not indefinite. The Court construes "said second oxidation layer" to mean "said second oxide layer."

7. "the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate" (claims 6, 7, 9, 10 and 19)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary. If "contact resistance" should be explicitly construed, then it should be construed under its plain and ordinary meaning in light of the specification as "resistance between two contacts."	Indefinite

The Parties' Positions

The parties dispute (1) whether there is an indication of the amount of reduction needed to be "reduced," (2) the baseline against which the reduction is measured, (3) whether "size" is indefinite as to how it is measured (e.g., length, width, volume, etc.), and (4) whether the use of "or" is confusing.

KAIST contends Defendants' expert confirms a person of ordinary skill in the art would immediately understand the size of a contact is width multiplied by length. Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 21 (citing Subramanian Dep. [Dkt. # 93-3] at 216:13–24, 217:16–20). KAIST urges that the claim language allows for the size of contacts to be increased by increasing their length beyond the length of the gate, their width beyond the width of the fin active region, or both. *Id*. (citing Kuhn Decl. [Dkt. # 93-4] ¶¶ 120–21). KAIST notes Defendants' expert testified that one skilled in the art would readily understand the relationship between width, length, and contact resistance. *Id*. at 22 (citing Subramanian Decl. [Dkt. # 106-1] ¶¶ 81–82 ("a POSA would understand that contact resistance is inversely proportional to the cross-sectional area of the contact")). KAIST says this conforms to the specification: "the integration of a device can be improved and

the contact resistance can be reduced by constructing the size of the contact region 46, which is in contact with said metal layer 48, wider than the width of the Fin active region and longer than the length of the gate 16." '055 Patent at 5:58–62. KAIST also notes Defendants' IPR expert referred to "the length ('size') of the source/drain contact region ('contact region') which is in contact with the contact plug 28 ('metal layer') [to be] greater than the width of the fence 313 (analogous to the 'Fin active region' in *Inaba*), as the width of the contact hole 27 is made wider than the width of the fence 313." *Id.* at 22 (citing Bokor Decl. [Dkt. # 93-12] ¶ 111).

Defendants first argue "reduced" is a term of degree for which the specification provides no guidance. Without a baseline, a person of ordinary skill in the art is not informed of objective boundaries for determining whether "contact resistance is reduced." Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 25.

Defendants next contend the specification does not provide sufficient guidance on how to measure the size of the contact region—that is, whether it should be measured by its length, width, area, or volume, depending on its shape. *Id*. Defendants contend the claim language underscores the lack of clarity by expressly requiring this "size" be "greater than the width of said Fin active region and/or the length of said gate." This is confusing because, as KAIST admits, it is the area that determines the "size of a contact region." *Id*. at 25–26. Defendants note that in the only instance in which the '055 Patent refers to "contact resistance" being "reduced," the specification discloses "the size of the contact region" as "wider than the width of the Fin active region and longer than the length of the gate"—not wider than the width of the fin active region "or" longer than the length of the gate. *Id.* at 26 (quoting '055 Patent at 5:58–62). Thus, the "and/or" portion of the claim term ultimately results in a nonsensical meaning because a POSA would have understood the reduction of contact resistance can only be determined by the area of the contact. *Id*.

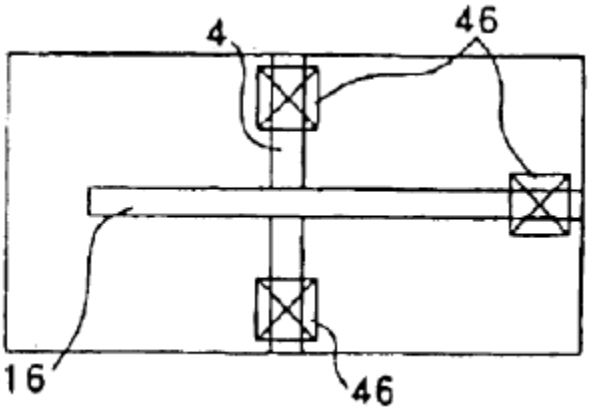
(citing Subramanian Decl. [Dkt. # 106-1] ¶¶ 149–55, 160–61). KAIST contends there is no sensible or realistic construction if the additional "or" term is also operative, as expressly recited in the claim.

KAIST replies the claims provide that contact resistance is reduced by selecting the size of the contact region within a certain parameter. KAIST contends Defendants do not dispute that one of skill in the art would understand selecting the size of a contact region or have the skill to test whether a given design results in reduced resistance. Pl.'s Reply Br. [Dkt. # 113] at 9. As to the use of "or," KAIST contends one of skill in the art would understand how to make all alternatives operative. *Id.* (citing Kuhn Decl. [Dkt. # 93-4] ¶¶ 119–26).

Analysis

The term "reduced" is like the terms above in that the claims do not require a specific *amount* of reduction. Rather, the claim only requires a reduction.

As to a reference for the reduction, the claims and specification make this clear. The contacts 46 to the fin active region 4 and the gate 16 may be larger than the fin active region 4 and gate 16.



'055 Patent fig.6c, 5:58–62 7:39–54. As is apparent in the figure and the specification, the contacts 46 have a width "wider than the width of the Fin active region" and a length "longer than the length

of the gate 16." *Id*. at 5:58–62. Further, "the contact resistance can be reduced by constructing the size of the contact region 46, which is in contact with said metal layer 48, wider than the width of the Fin active region and longer than the length of the gate 16." *Id*. In light of the specification, the patent is clearly comparing the contact to the Fin active region 4 to the width of the Fin active region 4. Moreover, the reference to which the contact to the gate 16 is being compared is the length of the gate 16. Increasing the contact area provides improved contact resistance. Thus, the specification itself rebuts Defendants' argument that there is no "baseline." The cited expert testimony of the three experts also better conforms to this understanding.

As to contact resistance, the experts agree the surface area of the connection between the two conductors affects that resistance. Whether this surface area is changed by length or width does not render the term indefinite. This also conforms to the dimensional nature of contact resistance as described in the specification. '055 Patent at 5:58–62, 5:63–66.

As to the "or" issue, the claims themselves provide guidance. The claims first recite a contact region and metal layer formed at the source/drain and gate contact region. The claims then recite that the contact resistance is reduced by sizing the contacts with reference to the fin active region "and/or" the gate. Thus, the claims make clear that either the contacts 46 to the fin active region, the contact 46 to the gate, or the contacts to both the fin active region and the gate may be sized to obtain the resistance reduction. The use of "or" simply allows for the contact to just the fin active region or the contact to just the gate to be sized in such a manner.

The Court finds "the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate" is not indefinite and has its plain and ordinary meaning.

* * *

8. "said selective epitaxial layer is grown by depositing a dielectric layer, and anisotropically etching as much as the thickness of the dielectric layer and the height of the Fin active region protruding above the second oxide layer, and taking the silicon which is exposed at side-walls of the Fin active region except the vicinity where the Fin active region and gate meets and a poly-silicon gate, as seeds" (claims 9 and 19)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary.	This claim element is a product-by-process limitation. This claim element is indefinite.

The Parties' Positions

The parties dispute whether "vicinity" renders the term indefinite. KAIST contends "vicinity" is given context in that a thin sidewall spacer of dielectric is formed on the gate and the thickness of this sidewall spacer gives reference to the use of "vicinity." KAIST claims the "vicinity" language therefore teaches a person of skill in the art that the epitaxial layer will either be grown up to the gate (when there is no spacer on the gate sidewall) or grown up to the spacer surrounding the gate (when there is spacer present). Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 25. According to KAIST, Defendants' expert admits the patent discloses a spacer embodiment and that a person of skill in the art would understand that, if a spacer is present, the epitaxial layer would only grow up to the location of the spacers, which are on either side of the gate. *Id*. (citing Subramanian Dep. [Dkt. # 93-3] at 150:13–23, 140:24–151:13, 151:23–152:15, 155:23–156:5, 158:5–16, 159:8–11, 160:7–9).

KAIST contends the specification describes a well-known spacer process that deposits a dielectric layer over the gate and then utilizes an anisotropic etch to leave a thin dielectric layer (the "spacer") on the sidewalls of the gate. Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 24 (citing Kuhn Decl. [Dkt. # 93-4] ¶ 132 (citing '055 Patent at 7:23–24 ("a dielectric layer with thickness

between 5 nm and 100 nm is deposited"); *id.* at 7:24 ("anisotropic etching is carried out"))). The spacer is intended to protect "the vicinity where the gate 16 comes into contact with source/drain Fin active region 4" from epitaxy. *Id.* (citing '055 Patent at 7:29). KAIST contends the height and thickness of the spacers can be controlled by the details of the etch process, which permits some tailoring of the size of the exposed fin active region for the epitaxy, as would be well understood by a person of skill in the art. Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 24–25 (citing Kuhn Decl. [Dkt. # 93-4] ¶ 134). KAIST contends a person of skill in the art would have readily understood the vicinity where the fin active region and gate meet cannot be used as a seed to grow the epitaxial layer because the residual oxide (spacer) from the anisotropic etch process remains and no silicon surface on the fin active region is exposed. *Id.*

Defendants, on the other hand, claim "the vicinity where the Fin active region and gate meets" renders the term indefinite. According to Defendants, this element specifies the location of the fin active region sidewalls used as a "seed" for "selective epitaxial layer grow[th]," and that they are used as such seeds except in the "vicinity where the Fin active region and gate meets." Defendants contend "vicinity" is an imprecise term not commonly used in the semiconductor manufacturing field, where precision is required. Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 27 (citing '055 Patent at 7:22–29).

KAIST replies that, other than asserting that "vicinity" is not commonly used in the semiconductor manufacturing field, Defendants fail to articulate exactly what makes this term unclear and fail to address the disclosure of the dielectric deposition and anisotropic etch disclosed in the specification. Pl.'s Reply Br. [Dkt. # 113] at 9.

Analysis

Although "vicinity" is only used once in the patent and is not a term typically used in the

semiconductor field, the specification provides guidance as to formation of the dielectric layer in the vicinity where the gate and source/drain fin active regions meet, ’055 Patent at 7:22–29, and how the “exposed Fin active region” is used as a “seed,” *id*. at 7:30–32. The “exposed Fin active region” is used in contrast to the regions covered by the dielectric layer. The thickness of the remaining sidewall deposition is implied through the description of the etch as being anisotropic, but limited to the thickness of the deposition and the height of the fin active region. Further, the specification describes an exemplary dielectric layer thickness of 5 nm to 100 nm. *Id*. at 7:21–27. Thus, in context of the specification, the “vicinity” teaches the epitaxial layer will either be grown up to the gate when there is no spacer on the gate sidewall or grown up to the spacer surrounding the gate when there is spacer.

The Court finds “said selective epitaxial layer is grown by depositing a dielectric layer, and anisotropically etching as much as the thickness of the dielectric layer and the height of the Fin active region protruding above the second oxide layer, and taking the silicon which is exposed at side-walls of the Fin active region except the vicinity where the Fin active region and gate meets and a poly-silicon gate, as seeds” is not indefinite. The Court finds “the vicinity where the Fin active region and gate meets” means “within the width of the dielectric layer, if any, on the sidewall of the gate, where the Fin active region and gate meet.”

* * *

9. "said doping junction depth for the source/drain formed in said Fin active region when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to 50 nm above the reference level" (claim 11)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary.	Indefinite

The Parties' Positions

The parties raise two issues. First, does use of "around" render the term indefinite? Second, does the use of "said" render the term indefinite because "doping junction depth" is not recited elsewhere?

KAIST contends the meaning of "doping junction depth" is well-known in the art and readily understood in light of the claims and specification. Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 26. KAIST further contends a person of ordinary skill would be well aware of the complexity of fabricating a transistor and know how to use manufacturing tolerances associated with the location of the doping junction to understand "around." *Id.* at 26 (citing Kuhn Decl. [Dkt. # 93-4] ¶¶ 139–40). KAIST contends courts have routinely held that such terms are definite. *Id.* (citing cases). KAIST notes Defendants' expert admitted a person of skill in the art would understand that "about" means the known manufacturing tolerance associated with a doping process, *id*. at 26–27 (citing Subramanian Dep. [Dkt. # 93-3] at 235:18–24, 236:2–8, 236:17–237:14), and that his declaration is conclusory as to why one skilled in the art would have trouble understanding this term. KAIST also contends Defendants' IPR expert contradicts Subramanian by explaining a person of skill in the art would have understood "around" as an approximation of a range of locations with equivalent behavior. *Id*. at 27 (citing Bokor Decl. [Dkt. # 93-12] ¶¶ 116–17; Kuhn Decl. [Dkt. # 93-4]

¶¶ 142–43).

In contrast, Defendants contend "said doping junction depth" lacks antecedent basis and its meaning is unclear. According to Defendants, even if a POSA were able to determine the meaning of "said doping junction depth," the additional limiting language "around 0 nm to 50 nm above the reference level" renders its scope unclear. Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 27. The '055 Patent only once refers to a "junction depth" being above a "reference" line, and in that instance does not use "around" to describe the location of the junction depth. Defendants contend the '055 Patent merely states the "junction depth should be lie [sic] in a range which is greater than 0 nm and less than 50 nm above the reference line." '055 Patent at 7:11–15.

As to KAIST's arguments about the imprecise manufacturing tolerances and the location of the junction, Defendants contend "around" further inflates the imprecision of these terms. Defendants contend the term is not "precise enough to afford clear notice of what is claimed." Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 28 (quoting *Nautilus*, 134 S. Ct. at 2129).

Analysis

The claim language calls out not just "said doping junction depth" but "said doping junction depth for the source/drain formed in said Fin active region." Earlier the claims recite "a source/drain region which is formed on both sides of the Fin active region." The specification also calls out the depth of the source/drain junction in the Fin active region. '055 Patent at 7:4–19. Thus, in context of the claims and the specification, the use of "said" causes no ambiguity.

Further, statements of the competing experts better support KAIST's position when viewed in the context of the intrinsic record. The usage of "said" does not create confusion in that, as claimed and described, the doping junction depth is for the source/drain formed in said fin active region.

As to the dispute about whether "around" is indefinite, the Federal Circuit has found that such terms do not inherently render a term indefinite. *See Allergan, Inc. v. Teva Pharma. USA, Inc.*, No. 2:15-CV-01455-WCB, 2016 WL 7210837, at *12, *15–16 (E.D. Tex. Dec. 13, 2016) (Bryson, C.J.) (providing a detailed review of the law in the context of the similar term "about"). *Allergan*'s rationale applies to "around," which is used in a manner similar to "about." Further, the nature of the technical field and the understanding of one skilled in the art may be used to provide guidance. *See Eibel Process Co*, 261 U.S. at 65; *Modine Mfg. Co.*, 75 F.3d at 1554; *Pall Corp.*, 66 F.3d at 1217; *Andrew Corp.*, 847 F.2d at 821. The evidence of those skilled in the art makes clear that in this field exact junction depths are not the norm but rather manufacturing tolerances impact the junction depth formation such that approximations are used. *See* Kuhn Decl. [Dkt. # 93-4] ¶¶ 139–40; Subramanian Dep. [Dkt. # 93-3] at 235:18–24, 236:2–8, 236:17–237:14; Bokor Decl. [Dkt. # 93-12] ¶¶ 116–17. The Court finds this extrinsic evidence more persuasive than Defendants' arguments. *See Teva Pharm. USA*, 135 S. Ct. at 841 (2015) (allowing courts to make subsidiary factual findings about the extrinsic evidence).

Accordingly, the Court finds "said doping junction depth for the source/drain formed in said Fin active region when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to 50 nm above the reference level" is not indefinite and that the term has its plain and ordinary meaning.

* * *

10. "said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to -50 nm below the reference level" (claim 12)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary.	Indefinite

The parties raise three issues: (1) Is the use of "around" indefinite? (2) Does the use of "said doping junction depth" render the term indefinite because "doping junction depth" is not recited elsewhere? (3) Is the use of "-50 nm below" indefinite (i.e., is a negative number "below" the same as a positive number above)?

The Parties' Positions

As to the issues of "around" and "said," the parties rely on the arguments presented above for the prior doping junction term. As to "below," KAIST contends the specification expressly teaches placing the doping junction below the reference line and the resulting benefits: "When the upper surface of the second oxidation layer is taken as a reference line, the junction depth should be lie [sic] in a range . . . less than 0 nm and greater than -50 nm [so] the current driving capability is improved . . . ." '055 Patent at 7:11–18.

As for the meaning of "-50 nm below," Defendants contend there are multiple interpretations, and that it is not reasonably clear whether this term means "50 nm below" or "50 nm above." Defs.' Resp. Cl. Constr. B. [Dkt. # 106] at 29 (citing Subramanian Decl. [Dkt. # 106-1] ¶ 183)). Defendants contend the specification only refers to a "junction depth" being "below" a "reference" line once, and in that instance indicates the junction depth is in a "range . . . less than 0 nm and greater than -50 nm" above the reference line. Defendants note "-50 nm below" does not appear

in the specification.

Analysis

For the same reasons discussed *supra* for the prior "said doping junction term," the Court rejects Defendants' indefiniteness arguments as to the use of "around" and the antecedent basis of "said doping junction depth."

As to the "-50 nm below" issue, the specification provides two examples of the junction depth. The upper surface of the second oxidation layer is used as the reference level. '055 Patent at 7:11–18. This is clear in the claim itself, which recites "the upper surface of said second oxide layer is taken as a reference level (0 nm)." The specification also makes clear the junction depth may be above the reference line and that, in another embodiment, the junction depth may be below the reference line:

> When the upper surface of the second oxidation layer 10 is taken as a reference line, the junction depth should be lie in a range which is greater than 0 nm and less than 50 nm above the reference line in order to suppress the short channel effects.
>
> On the contrary, if the range is less than 0 nm and greater than -50 nm then the current driving capability is improved rather than suppressing the short channel effects.

'055 Patent at 7:11–18.

Clearly, the junction depth can be at a level of -50 nm (the surface of the second oxidation layer being a reference level), which is below the reference layer. Interpreting "below" to actually refer to a condition of being above the surface of the second oxide layer is unreasonable in light of the specification. Thus, in the context of the specification, no further construction is needed and the Court finds the term is not indefinite.

The Court finds "said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is

around 0 nm to -50 nm below the reference level" has its plain and ordinary meaning.

* * *

11. "the oxidation layer" (claim 13)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary. If this claim term should be explicitly construed, then it should be construed under its plain and ordinary meaning in light of the specification as "second oxide layer."	Indefinite

The Parties' Positions

The parties dispute whether the term is indefinite because "the oxidation layer" lacks an antecedent basis. KAIST contends one skilled in the art would readily understand "the oxidation layer" refers to the previously recited "second oxide layer." As discussed *supra* with respect to the "first oxidation layer" and "second oxidation layer," KAIST contends the specification uses "oxidation layer" interchangeably with "oxide layer," for which antecedents appear in the claim. Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 28.

KAIST notes the surrounding language of the limitation states "wherein the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate." This, says KAIST, describes an "oxidation layer" adjacent to the bulk substrate and through which the fin active region passes as it connects to the substrate. KAIST contends the preceding claim limitations make clear the second oxide layer is the layer which is adjacent to the substrate. *Id.* at 28–29. KAIST further contends the specification also makes clear the fin active region passes through the second oxide layer as it widens and connects with the bulk substrate. *Id.* at 29 (citing '055 Patent figs.12d & 13d, 5:54–63). KAIST

notes this is consistent with Defendants' IPR expert's interpretation. *Id*. (citing Bokor Decl. [Dkt. # 93-12] at ¶ 120).

Defendants, however, contend the term is indefinite because "the oxidation layer" has no antecedent basis. Defendants contend Claim 13 recites multiple "oxide layers"—"a gate oxide layer," "a first oxide layer," "a second oxide layer"—but no "oxidation layer" is previously recited. Defendants contend that, given "oxide layer" has a different meaning than "oxidation layer," this element is susceptible to multiple interpretations. Defs.' Resp. Cl. Constr. Br. [Dkt. # 106] at 29 (citing Subramanian Decl. [Dkt. # 106-1] ¶¶ 200–07). Moreover, Defendants contend one skilled in the art would have understood "oxidation layer" to mean "layer formed by oxidation," a well-known process in which a material is exposed to oxygen to form an oxide. *Id*. Defendants claim "oxide layer" means a "layer that is oxide," but not a layer necessarily one formed by "oxidation." Thus, Defendants contend "oxidation layer" and "oxide layer" have different meanings. *Id*.

The parties did not provide argument for this term at the oral hearing. H'rg Tr. (Dec. 13, 2017) [Dkt. # 161] at 103–04.

Analysis

The claim recites "the oxidation layer." Earlier the claim recites three oxide layers: a first oxide layer, a second oxide layer and a gate oxide. The claim itself describes the second oxide layer as being the oxide layer on the bulk silicon substrate, and the disputed term includes the limitation "as it approaches the bulk silicon layer." As the first oxide layer is formed on the top of the fin and the gate oxide is formed on the sides of the fin (above the second oxide), only an interpretation of "the oxidation layer" being the "second oxide layer" makes sense in light of the other claim limitations.

That interpretation conforms to the only embodiment of the specification, which teaches

that the resistance of the fin active region is reduced by enlarging the width of said fin active region within the oxidation layer as it approaches the bulk silicon substrate. '055 Patent at 5:63–67. Likewise, Figures 12d and 13d illustrate the width of the fin active region becoming enlarged as it approaches the bulk silicon substrate. In each case, it is the oxide layer on the bulk silicon (the claimed second oxide layer) within which the enlarging occurs.

In context of the claims and the specification, the only reasonable interpretation of "the oxidation layer" is a reference to the earlier recited "a second oxide layer." The Court therefore construes "the oxidation layer" to mean "the second oxide layer."

* * *

12. "the top two corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere" (claim 15)

KAIST's Proposed Construction	Defs.' Proposed Construction
This claim term is definite and has a plain and ordinary meaning. No construction is necessary, but if this claim term should be explicitly construed, then it should be construed under its plain and ordinary meaning in light of the specification as "and/or"	This claim element is a product-by-process limitation. This claim element is indefinite.

The Parties' Positions

The parties dispute whether the use of "or (and)" renders the term indefinite. KAIST contends one skilled in the art would readily understand the chamfering is achieved through (1) an oxidation and etching process, or an annealing process, or through (2) oxidation, etching, and annealing. Pl.'s Opening Cl. Constr. Br. [Dkt. # 93] at 30 (citing Kuhn Decl. [Dkt. # 93-4] ¶¶ 161–62). KAIST notes neither of Defendants' experts supports Defendants' contention of indefiniteness, because Dr. Bokor had no trouble understanding and applying the claim term in the IPR

proceedings and Dr. Subramanian was silent on the claim term. *Id*. KAIST contends Defendants merely provide a conclusory statement without evidence, which does not meet Defendants' indefiniteness burden. Pl.'s Reply Br. [Dkt. # 113] at 10.

Defendants contend the claimed feature recites a fin active region having chamfered top two corners formed by the process steps of (1) oxidation and etching, or (and) (2) annealing process in a hydrogen atmosphere. Defendants contend that without any substantive discussion of this phrase in the specification, and given its use of "or (and)," this phrase is indefinite. Defs.' Resp. Cl. Constr. Br. [Dkt. #106] at 30.

The parties did not provide argument for this term at the oral hearing. H'rg Tr. (Dec. 13, 2017) [Dkt. # 161] at 103-04.

Analysis

Defendants point to no evidence the term is indefinite. As described in the specification, (1) oxidation and etching *and* (2) annealing may be done. The specification, however, indicates that alternatively, (1) oxidation and etching *or* (2) annealing may be done. Though use of "and/or" or "or/and" may be more commonplace, in context of the intrinsic record, the claim's use of "or (and)" provides reasonable certainty as to the scope of the claim in conformance with the specification. This also conforms to the only evidence of one skilled in the art presented by the parties. *See* Kuhn Decl. [Dkt. # 93-4] ¶¶ 161–62.

The Court finds "the top two corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere" is not indefinite. The Court finds "or (and)" means "and/or."

Order

The Court adopts the constructions set forth *supra* for the disputed terms. The parties may

not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties must refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

SIGNED this 2nd day of February, 2018.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE